

RF Post-Layout Performance Prediction with Deep Learning and Image Processing

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Abstract—As a significant barrier in the design cycle, post-layout simulation has remained a major bottleneck in analog or radio frequency (RF) circuit design due to its high computational cost. In this paper, we propose an effective solution to post-layout performance prediction by estimating key metrics without time-consuming simulations. This challenge is particularly critical in RF circuits, where parasitic effects strongly affect circuit performance. We develop a deep learning (DL) framework for RF post-layout performance prediction, explicitly accounting for component location and routing variations. A dataset of 1,132 low-noise amplifier's (LNA) layouts is constructed, and an adapted DenseNet-121 model, fine-tuned via transfer learning, is employed for our generated dataset. The proposed model outperforms its benchmark ResNet-50 and ResNet-101 in both classification and regression tasks. For classification, DenseNet-121 achieved an accuracy of 98.23% for forward gain (s_{21}) and 97.35% for noise figure (NF). Meanwhile, regarding regression, it delivered an R^2 value of 0.98 and 0.88 for s_{21} and NF, respectively.

Index Terms—Post-layout simulation, performance prediction, radio frequency (RF), placement and routing, and deep learning

I. INTRODUCTION

Advancements in the fifth generation (5G) networks, Internet of Things (IoT), and high-speed computing demand complex, high-performance integrated circuits (ICs). While automation has streamlined digital IC design, analog/RF layout remains a time-consuming, labour-intensive process. Due to strong impact of layout parasitics [1], process variations [2], device matching as well as symmetry [3], analog/RF layout design still relies heavily on expert knowledge and iterative adjustments, which might result in prolonged design cycles. To address challenges from perpetual technology scaling and growing circuit complexity, analog/RF layout automation becomes essential to enhance design efficiency and overcome layout bottlenecks [4].

Indeed, automation in analog/RF layout has been an active area of research in recent years. Considering fully automated layout generation, recent ALIGN [5] and MAGICAL [4] are prime examples for open-source frameworks that translate a circuit netlist to a complete layout, advanced from the conventional procedure layout tools [6]. Besides full-layout generation, significant efforts have also focused on automation of subproblems such as placement and routing, especially by using advanced artificial intelligence (AI) methods. In [7], a reinforcement learning (RL)-based placement method was proposed, in which an artificial neural network (ANN) agent was trained to control the fogging effect. Meanwhile, HyperPlace, introduced by [8], leveraged the state-of-the-art large language model (LLM) to automate hyperparameter tuning in GPU-accelerated placement tools. In addition, GeniusRoute

[9] employs a variational auto-encoder (VAE) to learn and apply manual routing patterns in automatic detailed routing.

Despite these advances, automated layout generation alone might not guarantee optimal analog/RF circuit performance, which is highly sensitive to parasitics and process variations. While traditional post-layout simulations provide accurate performance metrics, they are computationally expensive and can significantly slow down the design cycle [4]. To address this, post-layout performance modeling, similar to circuit behavior [10], has emerged as a means to predict key design metrics. This operation promises to enable circuit evaluation without repeatedly performing time-intensive parasitic extraction and post-layout simulations.

In early efforts, abundant schematic-level samples were utilized as inputs to train an ANN model, which was then fine-tuned on a limited set of post-layout samples using transfer learning techniques [11]. This approach allows designers to benefit from large amounts of low-cost schematic data to adapt to post-layout information. However, the major limitation of this method is that layouts used to generate post-layout data must be highly regular, since the input to the transferred models contains only sizing-related parameters without detailed layout information available.

To address the shortcoming related to post-layout data, recent research has employed convolutional neural networks (CNNs) to directly process layout images, which can capture rich spatial and structural layout features for more accurate post-layout performance prediction. In [12], a 3D CNN was proposed to predict the relative placement quality on post-layout performance, primarily focusing on the classification task. The work of [1] later extended this approach to address the regression problem and predict post-layout performance metrics rather than only classifying layout quality. All of these studies [12], [1] are built upon datasets of low-frequency operational transconductance amplifiers (OTAs) layouts that primarily consider layout placement. This has called upon two research gaps as highlighted below. First, low-frequency designs are generally less sensitive to layout variations compared to RF circuits, clearly a gap in post-layout performance prediction models for RF designs. Secondly, these methods mainly rely on placement information, while routing, which also plays an important role in determining post-layout performance, remains largely unmodelled.

In this paper, the two aforementioned gaps in post-layout performance prediction are addressed. The key contributions of our research include:

- 1) This study extends beyond placement prediction by modeling routing information to better capture its impact

on post-layout circuit behavior. We develop an image-processing-based approach where routing and via geometries are represented as multi-channel images, which leverages developed computer vision techniques to facilitate layout automation;

- 2) An LNA layout dataset is constructed to facilitate the need for RF layout dataset. In particular, our dataset is designed to capture routing impact on post-layout circuit performance. Essentially, this dataset was generated using the commercial tool Cadence Virtuoso, which ensures full function for RF layout generation - a critical capability that is not supported by open-source academic tools;
- 3) Both the classification and regression problems are studied for RF post-layout routing prediction. A transfer learning technique is employed for our DL model to alleviate the need for a large dataset and enhance the generalization and training efficiency.

The rest of the paper is organized as follows. Section II discusses the generation of the LNA layout dataset and corresponding data preprocessing steps. Section III outlines the implementation of DL model to predict LNA's key performance metrics based on the proposed routing-aware layout image dataset. Section IV presents our experimental results, while Section V concludes this paper.

II. DATASET AND FEATURE ENGINEERING

This section describes the process of constructing the LNA layout dataset with its key performance metrics. This is followed by corresponding feature engineering steps to facilitate effective model training.

A. Low-Noise Amplifier (LNA)

LNAs are key components in RF front-end systems, providing signal amplification while minimizing noise. As the first active stage in the signal chain, LNAs strongly influence the receiver's sensitivity and linearity. Among critical design metrics, forward gain (s_{21}) and noise figure (NF) indicate amplification and noise performance, respectively. Accurate post-layout prediction of these parameters is challenging because they are sensitive to parasitics, coupling, and device proximity. This highlights the need for data-driven models to capture the complex relationship between layout and performance.

B. Data Generation

To develop a data-driven post-layout performance model, a Cascode inductive-degenerated LNA operating at 5.6 GHz was implemented in the TSMC 65nm CMOS technology. Its schematic, used for dataset generation, is shown in Fig. 1.

The dataset was generated using the commercial layout tool Cadence Virtuoso, which offers full function for RF layout generation. This functionality is absent in open-source academic tools such as ALIGN [5] and MAGICAL [4], which currently do not support inductor layout generation. Cadence Virtuoso was selected by virtue of its dominant, industry-standard role for custom (mainly analog, RF and mixed-signal) IC design. Moreover, it is worth mentioning that, as a commonly accepted norm, high-accuracy industry-strength simulation tools are generally considered as a primary proxy to the silicon chip fabrication/measurement in the EDA research when developing IC computer-aided design (CAD) algorithms or tools.

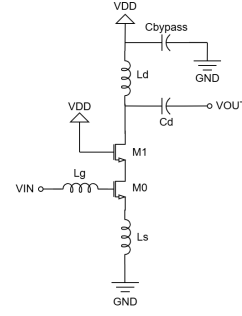


Fig. 1: Schematic of the LNA circuit for dataset generation

The dataset is designed to specifically examine how routing variations affect circuit performance. To achieve this, the placement of all circuit components is fixed across all samples, and only routing is modified. This setup allows a focused investigation of routing effects on s_{21} and NF. Furthermore, all layout samples are required to pass the standard verification checks, including design rule check (DRC) and layout versus schematic (LVS) check performed by Siemens Calibre, prior to parasitic extraction and post-layout simulation.

A total of 1,132 layout samples are generated using the Custom/Digital Routing Flow in the Cadence Virtuoso Space-Based Router by systematically varying wire width, routing style, via counts, and routing penalty. For each sample, to isolate routing effects, only routing and via layers are exported as images, with device placement hidden. These images are paired with their corresponding post-layout s_{21} and NF to facilitate model training and evaluation.

Performance labels are derived from Cadence Virtuoso post-layout simulations. Across the 1,132 generated samples, s_{21} ranges from -24.89 dB to 17.69 dB with mean $\mu = 5.01$ dB and standard deviation $\sigma = 12.79$ dB, while NF ranges from 2.25 dB to 20.19 dB with $\mu = 4.68$ dB and $\sigma = 3.71$ dB.

C. Feature Engineering

To ensure data integrity, layout geometries are constrained by minimum width and spacing rules to prevent aliasing or merging during rescaling. Non-geometric features, such as net names and patterns, are removed to minimize input noise. Each layer is assigned a unique RGB intensity before being flattened into a grayscale representation, preserving distinct layer-wise features for the DL model.

The exported 2D layout images are rescaled to 512 x 512 pixels, which provides a good balance between preserving detailed routing information and maintaining manageable computational cost. Subsequently, the images are converted to grayscale to standardize the CNN input and further reduce complexity. Fig. 2 shows a comparison between an LNA layout image with devices' placement and routing, and, an LNA layout image with only routing.

III. DEEP LEARNING MODEL IMPLEMENTATION FOR IMAGE PROCESSING

This section describes the DL framework, namely DenseNet-121, for our prediction problem. It covers all the steps to build and adapt DenseNet-121 to our LNA layout images to predict post-layout s_{21} and NF.

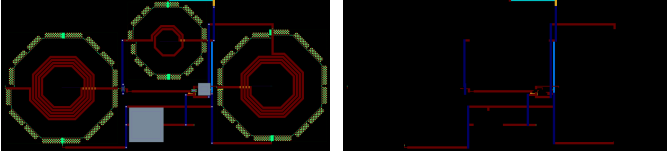


Fig. 2: Comparison between an LNA full layout image versus an LNA layout image with only routing

A. Model Selection

CNNs excel in image recognition by capturing hierarchical spatial features through convolutional operations. A typical CNN combines convolutional and pooling layers for feature extraction and downsampling, followed by fully connected layers for prediction. However, as CNNs become deeper, they may suffer from vanishing gradients and parameter inefficiency, which limit scalability and training stability [1].

To address these challenges, this study employs DenseNet-121, a 121-layer architecture organized into dense blocks, where each layer receives inputs from all preceding layers to promote feature reuse and efficient gradient propagation. DenseNet-121 maintains a compact number of parameters while achieving high performance on large-scale benchmarks such as ImageNet. Its ability to preserve multi-scale spatial information makes it well-suited for learning subtle routing patterns that influence post-layout circuit performance.

B. Model Adaptation and Training

To adapt DenseNet-121 for layout performance prediction, the input layer is reconfigured from the standard three-channel format to a 21-channel, 512x512 stacked grayscale representation corresponding to 21 routing and via layers. The first convolutional layer is reinitialized to accommodate this dimensionality, while pretrained ImageNet weights are transferred to remaining layers to leverage prior feature representations and accelerate convergence.

For model development, the dataset is divided into 80% for training, 10% for validation, and 10% for testing. The model is trained using the Adam optimizer with a learning rate of 0.0001 and a batch size of 32.

C. Transfer Learning Strategy

In this study, transfer learning is applied by initializing DenseNet-121 with pretrained ImageNet weights, with the first convolutional layer reinitialized to accommodate the 21-channel layout image input. This approach allows the network to utilize generic feature representations learned from large-scale natural images while adapting to the domain-specific task of post-layout performance prediction with a relatively small LNA layout dataset (1132 samples).

IV. EXPERIMENTAL RESULTS

This section discusses the training, validation and testing results using DenseNet-121 model, implemented with 60% of pretrained weights from ImageNet, on our layout routing image dataset versus those from ResNet-50 and ResNet-101. All models' training, validation and testing were performed on a Windows system featuring an Intel 2.1 GHz i7-14700 CPU, 16 GB of RAM and an NVIDIA RTX A4000 GPU.

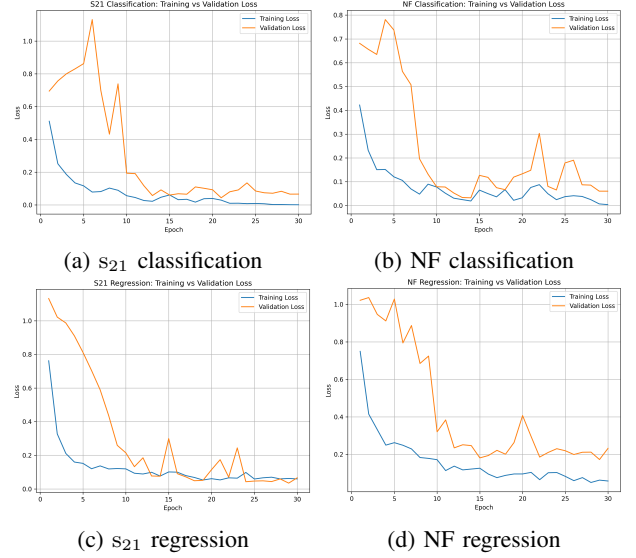


Fig. 3: DenseNet-121 model's training versus validation loss

A. Classification Problem

The classification task serves as a fast filter to determine if a layout meets specific performance thresholds, specifically $s_{21} > 10$ dB and $NF < 3$ dB for good samples in our study. This allows for the rapid removal of non-compliant designs without calculating exact values. Once a layout is verified as compliant, the regression model is then used to predict precise metrics for further optimization.

To evaluate our model, the metrics such as Accuracy, Precision, Recall and F1 score are used. The formulas for these metrics are defined as

$$\text{Accuracy} = \frac{TP + TN}{TP + TN + FP + FN}, \quad (1)$$

$$\text{Precision} = \frac{TP}{TP + FP}, \quad (2)$$

$$\text{Recall} = \frac{TP}{TP + FN}, \quad (3)$$

$$F1 = \frac{2 \times \text{Precision} \times \text{Recall}}{\text{Precision} + \text{Recall}}, \quad (4)$$

where TP, TN, FP, FN are true positive, true negative, false positive, and false negative values, respectively.

Fig. 3a and 3b compare the classification training and validation loss of s_{21} and NF. As shown in both figures, over the epochs, the gap between training and validation gradually decreases with slight fluctuation. To present the results numerically, after 30 epochs, the training loss and validation loss of s_{21} reach 0.0009 and 0.0690, respectively. Meanwhile, the loss values of NF settle at 0.0037 and 0.0601.

Table I further evaluates our DenseNet-121 model's performance on the testing set versus ResNet-50 and ResNet-101 as two other established models. For simplicity, the columns corresponding to DenseNet-121, ResNet-50 and ResNet-101 are renamed as Dense121, Res50 and Res101, respectively. According to Table I, DenseNet-121 outperforms its two counterparts regarding both s_{21} and NF. All four evaluation metrics for DenseNet-121 exceed 95%, justifying our choice of model for the post-layout performance prediction problem.

TABLE I: Performance comparison on the testing set of different models for the classification problem

Metrics	s_{21}			NF		
	Dense121	Res50	Res101	Dense121	Res50	Res101
Accuracy (%)	98.23	92.03	88.49	97.35	84.07	85.84
Precision (%)	96.07	88.46	80.00	98.21	76.00	84.75
Recall (%)	100.00	93.87	97.95	96.49	100.00	87.72
F1 score	0.98	0.91	0.88	0.97	0.86	0.86

TABLE II: Performance comparison on the testing set of different models for regression problem

Metrics	s_{21}			NF		
	Dense121	Res50	Res101	Dense121	Res50	Res101
MAE (dB)	0.23	2.30	4.49	0.71	0.85	1.29
RMSE (dB)	0.32	3.79	5.88	1.26	1.74	1.88
R^2	0.98	0.90	0.76	0.88	0.77	0.74

B. Regression Problem

To ensure faster and more stable convergence, z-score standardization is applied to s_{21} and NF on their dB scale to obtain a scaled dataset with $\mu = 0, \sigma = 1$.

In terms of the regression problem, we employed mean squared error as the loss function for our DenseNet-121 model. Furthermore, the evaluation metrics, including mean absolute error (MAE), root mean squared error (RMSE) and R^2 , are chosen with the given formulas below

$$MAE = \frac{1}{n} \sum_{i=1}^n |\hat{y}_i - y_i|, \quad (5)$$

$$RMSE = \sqrt{\frac{1}{n} \sum_{i=1}^n (\hat{y}_i - y_i)^2}, \quad (6)$$

$$R^2 = 1 - \frac{\sum_{i=1}^n (\hat{y}_i - \bar{y})^2}{\sum_{i=1}^n (y_i - \bar{y})^2}, \quad (7)$$

where y_i is the actual value, $\hat{y}_i$ is the predicted value of y_i and $\bar{y}$ is the mean value of all y_i in the dataset.

Fig. 3c and 3d compare the regression training and validation loss of s_{21} and NF, respectively. Similar to the pattern of classification, the gap between training and validation loss continuously decreases throughout the training process. Meanwhile, NF still exhibits a bigger difference compared to that of s_{21} . The final loss values for training and validation for s_{21} regression problem are 0.0595 and 0.0662, while those values for NF are 0.0578 and 0.2324, respectively.

According to Table II, similar to the classification problem, DenseNet-121 still maintains its superiority over ResNet-50 and ResNet-101 for the regression problem. For s_{21} , DenseNet-121 achieves a much lower MAE (0.23 dB) and RMSE (0.32 dB) and also a solid R^2 (0.98) compared to the other two benchmark models. In terms of NF, although the performance gap between DenseNet-121 and its two counterparts shortens, DenseNet-121 still delivers the best and most consistent results (e.g., satisfactory R^2 of 0.88).

The proposed DenseNet-121 model achieves an inference time of less than 1 second, representing a massive speedup versus approximately 4 minutes for a standard industrial flow (including DRC, LVS, parasitic extraction and post-layout simulation) [10]. While data generation requires a one-time

computational investment (approximately 90 hours for 1,132 samples), the trained model enables real-time performance estimation, eliminating the post-layout verification and simulation bottleneck to facilitate rapid, iterative layout optimization.

V. CONCLUSION

In this study, we presented a DL framework for post-layout performance prediction of RF circuits, focusing on LNAs. By representing routing and via geometries as 21-layer grayscale images, the approach enabled CNN to capture spatial correlations between layout features and key performance metrics, including s_{21} and NF. The DenseNet-121 model, adapted for 21-channel inputs and fine-tuned via transfer learning, demonstrated superior performance compared to ResNet-50 and ResNet-101 in both classification and regression tasks. Results confirm that image-based DL can effectively predict post-layout performance while reducing reliance on time-consuming simulations. Future work might extend this approach to additional RF circuit types, expand the dataset with both placement and routing variation, and explore multi-task learning to improve prediction accuracy and generalization.

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