

Efficient Machine Learning-Driven RF Post-Layout Prediction via Bidirectional State-Space Vision Mamba

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Abstract—Accurate performance estimation of radio frequency (RF) integrated circuits after placement and routing (P&R) is essential for accelerating design cycles and ensuring post-layout reliability. This paper proposes a vision mamba (Vim)-based framework as a high-speed surrogate model for RF P&R performance prediction, specifically for Low-Noise Amplifier (LNA) layouts. Utilizing an RF-specialized dataset comprising 21-channel grayscale representations of routing and via layers, we benchmark bidirectional state space model (SSM) against transformer-based vision transformer (ViT) and CNN-based DenseNet-121. Unlike self-attention mechanism or localized kernels, our methodology leverages SSM with subquadratic-time complexity to maintain high modeling power with minimal overhead. Experimental results show Vim achieves a superior R^2 of 0.92 in noise figure regression. Most significantly, Vim consistently outperforms benchmarks in training time efficiency, achieving training speeds up to 5.5 and 6.5 times faster than ViT and DenseNet-121, respectively, providing a robust solution for RF layout performance prediction.

Index Terms—Post-layout simulation, performance prediction, radio frequency (RF), placement and routing, vision mamba (Vim)

I. INTRODUCTION

The transition to advanced CMOS nodes and the integration into complex microsystems (e.g., micro-electro-mechanical systems and microfluidics) has fundamentally changed the integrated circuit (IC) design landscape [1], [2]. To support high-performance requirements of the fifth generation (5G) networks and Internet of Things (IoT), modern ICs integrate billions of transistors, resulting in a design space where traditional manual methods might be no longer efficient [3]. While electronic design automation (EDA) has played an essential role for managing this complexity and ensuring commercial viability, its application remains inconsistent across design domains [4], [5]. Specifically, analog/radio frequency (RF) layout remains a highly manual, experience-driven bottleneck. Unlike digital circuits [6], analog/RF performance is sensitive to transistor configuration and modeling [7] as well as its physical implementation, where minor variations in parasitics [8], device matching [9], [10], and process [11] may lead to significant performance degradation. This lack of standardized automation results in repetitive, labor-intensive iterations to maintain circuit integrity, highlighting a critical need for automated methodologies to streamline the analog/RF design cycle [12].

Recent years have seen significant progress in analog/RF layout automation. Fully automated frameworks like ALIGN [13] and MAGICAL [12] have emerged to translate circuit netlists directly into complete layouts. Beyond full-layout generation, research has increasingly targeted specific subproblems using advanced artificial intelligence (AI). In [14], reinforcement learning was applied to placement control through ANN agents while HyperPlace [15] utilized large language

models to automate hyperparameter tuning in GPU-accelerated tools. Furthermore, GeniusRoute [16] employed variational auto-encoder (VAE) to learn and replicate manual routing patterns in automatic detailed routing.

Despite these advances, automated layout generation alone might not guarantee optimal analog/RF circuit performance, which is highly sensitive to parasitics and process variations. While traditional post-layout simulations provide accurate performance metrics, they are computationally expensive and can significantly slow down the design cycle [17]. While a single simulation run, including parasitic extraction and electromagnetic (EM) analysis, may only require few minutes [18], the cumulative time becomes substantial across the entire development cycle, not to mention simulation in a loop that has become increasingly more common in the modern design and optimization process. To address this, post-layout performance modeling has emerged as a means to predict key design metrics. This operation promises to enable circuit evaluation without repeated time-intensive parasitic extraction and post-layout simulations.

Early efforts in post-layout modeling trained models with abundant schematic-level data and fine-tuned them on limited post-layout samples through transfer learning [19]. This approach benefits from low-cost schematic data to adapt to post-layout information; however, this method is restricted by its reliance on sizing parameters alone and highly regular post-layout data, failing to account for detailed layout geometries [17]. To address this shortcoming, recent research has employed convolutional neural networks (CNNs) to directly extract spatial and structural features from layout images. For instance, [20] proposed a 3D CNN to classify layout placement quality, while subsequent works [9] and [21] extended this approach to address regression problems for predicting specific post-layout performance metrics. However, these studies [9], [20], [21] rely on datasets of low-frequency operational transconductance amplifiers (OTAs) layouts that focus primarily layout placement. This leaves two critical research gaps: first, the lack of models tailored for RF circuits, which are far more sensitive to layout variations; and second, the omission of routing information, which significantly impacts post-layout performance but remains largely unattended in existing literature.

To address these limitations, this paper introduces a post-layout performance prediction framework based on vision mamba (Vim). While CNNs struggle with global dependencies and traditional sequence models face high computational overhead, Vim leverages a bidirectional state space model (SSM) to achieve a global receptive field with linear complexity. This allows Vim to efficiently capture characteristics and complex routing patterns that localized kernels might overlook.

By treating layouts as sequences of visual tokens without the quadratic scaling issues of attention mechanisms, our approach provides a robust, scalable solution for RF post-layout performance prediction.

The key contributions of our research include:

- **Routing-aware post-layout performance prediction:** We develop an image-based framework that explicitly models routing and via geometries as multi-channel images. This captures intricate physical features necessary for accurate post-layout analysis, enabling computer vision techniques for analog/RF domain.
- **RF layout dataset:** To address RF data scarcity, we implement an LNA layout dataset capturing routing impacts on post-layout performance. Generated via a popular commercial EDA tool, it reflects RF industry-standard design rules and functionalities that are typically not supported by open-source academic tools.
- **Bidirectional state-space-based global sequence modeling:** We introduce Vim for LNA post-layout performance prediction. By utilizing a bidirectional state-space model, this approach captures global spatial dependencies with linear complexity and subquadratic-time computation compared to vision transformer (ViT), effectively modeling long-range parasitic interactions that traditional CNN-based architectures might overlook.

The rest of the paper is organized as follows. Section II describes LNA layout dataset generation and corresponding preprocessing steps. Section III details the implementation of the Vim model for the proposed routing-aware post-layout performance prediction. Section IV presents our experimental results, while Section V concludes the paper.

II. DATASET AND FEATURE ENGINEERING

This section describes the construction of the LNA layout dataset with its key performance metrics, followed by feature engineering steps for effective model training.

A. Low-Noise Amplifier (LNA)

As the primary stage in RF front-ends, LNAs strongly influence the receiver’s overall sensitivity and linearity [22]. Key metrics such as forward gain (s_{21}), representing amplification, and noise figure (NF), indicating noise performance, are highly sensitive to layout parasitics and coupling [23], [24]. Therefore, in this work, LNA serves as an ideal test case to evaluate prediction models to facilitate the high computational costs of iterative simulations.

B. Data Generation

To develop the data-driven model, a 5.6 GHz Cascode inductive-degenerated LNA, as shown in Fig. 1, was implemented in TSMC 65 nm CMOS technology. The dataset was generated using a popular commercial analog/RF EDA tool, specifically Cadence Virtuoso, which offers full function for RF layout generation. This functionality is absent in open-source academic tools such as ALIGN [13] and MAGICAL [12], which currently do not support inductor layout generation. Cadence Virtuoso was selected as the industry-standard environment for custom RF IC design, though any comparable commercial EDA solution would yield similar results. Furthermore, high-accuracy industrial simulation tools are established as reliable proxies for physical silicon measurement in EDA research, providing a robust foundation for developing and validating IC computer-aided design algorithms.

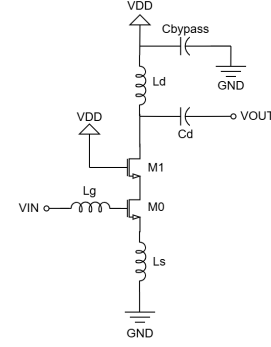


Fig. 1: Schematic of the LNA circuit for dataset generation

The dataset is designed to isolate the impact of routing on s_{21} and NF by fixing the placement of all circuit components across all samples and modifying only routing. Furthermore, all layout samples are required to pass the standard Siemens Calibre verification, including design rule check (DRC) and layout versus schematic (LVS), prior to parasitic extraction and post-layout simulation.

A total of 1,132 layout samples are generated using the Custom/Digital Routing Flow in the Cadence Virtuoso Space-Based Router [25] by systematically varying the preferred wire width on each metal layer, routing style, minimum number of via cuts, and the wrong-way routing penalty. For each sample, only the routing and via layers are exported as images, while device placements are intentionally hidden to isolate routing effects. These images are paired with their s_{21} and NF post-layout performance labels, derived from Cadence Virtuoso post layout simulations of industrial standard.

s_{21} and NF metrics serve as targets for a high-fidelity surrogate model to alleviate computational bottleneck of iterative post-layout verification. While the IC design community requires physical tapeout for validation, the EDA community widely accepts industry-standard simulations as a primary proxy for evaluating new design methodologies. Consequently, this framework complements the design flow rather than replacing final physical measurements of a chip tapeout.

C. Feature Engineering

To ensure data integrity, layout geometries are constrained by minimum width and spacing rules to prevent aliasing or merging during rescaling. Features such as net names and patterns are removed to minimize input noise. Each layer is assigned a unique RGB intensity before being flattened into a grayscale representation, preserving distinct layer-wise features for model training.

The exported 2D layout images are rescaled to 512 x 512 pixels, which provides a good balance between preserving detailed routing information and maintaining manageable computational cost. Subsequently, the images are converted to grayscale to standardize the CNN input and further reduce complexity. As illustrated in Fig. 2, a full LNA layout image shown on the left includes both electronic components and routing tracks, while a trimmed LNA layout image depicted on the right only encloses the routing tracks. In other words, this pipeline operation transforms a full LNA layout into a sanitized, routing-only representation for further processing.

III. VISION MAMBA FOR IMAGE PROCESSING

This section covers the architecture of the Vim model and its adaptation to prediction post-layout s_{21} and NF from our LNA layout image dataset.

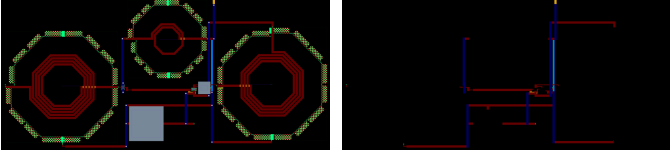


Fig. 2: Comparison between an LNA full layout image (on the left) versus an LNA layout image only with routing tracks (on the right)

A. Vim Model

The architectural components of Vim begin with the partition of a 2D input image into flattened 2D patches. A 2-D input image $x \in R^{H \times W \times C}$ is transformed into flattened 2D patches $x_p \in R^{J \times (P^2 \cdot C)}$, where (H, W) is the resolution of the original image, C is the number of channels, P is the size of image patches, and $J = HW/P^2$ is the number of patches. Then, x_p is linearly projected into vectors of a specific dimension, D . Because SSMS are sensitive to the order of the sequence, learnable position embeddings are added to these patch tokens to provide essential spatial awareness [26]. Additionally, a class token is prepended to the sequence, serving as a global representation of the entire image.

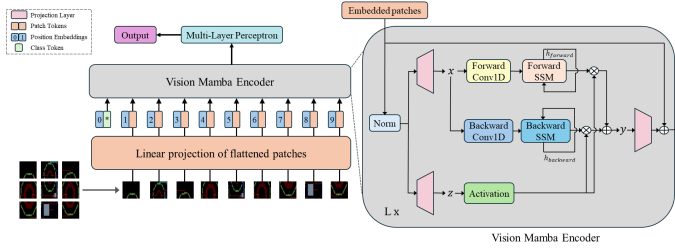


Fig. 3: Vim architecture

The main processing unit of the architecture is the Vim encoder, which consists of a stack of L identical blocks (Fig. 3). Each block utilizes a residual connection to ensure stability during training, where the output of each layer is added back to its input. Internally, the Vim block is designed to handle the bidirectional nature of visual data, which lacks the inherent causal order found in text [26]. The normalized input is projected into two branches, x and z , with a dimension size E . The x branch is processed through forward and backward 1-D convolutions for local context and then through forward and backward selective SSMS for global context. The z branch gates the bidirectional outputs, which are summed and projected back to dimension D . After L blocks, the class token is extracted, normalized, and processed by a multi-layer perceptron (MLP) head to generate the final output prediction.

B. Vim Adaptation and Training

To adapt Vim to our layout performance prediction task, the input layer is reconfigured to process 512×512 21-channel grayscale tensors. While these channels represent 21 routing and via layers in the layout dataset, the architecture can be scalable, allowing the channel depth to adjust dynamically to any change in the number of layers.

For model development, the dataset an 80/10/10 ratio for training, validation, and testing. Configured with a patch size of 16 and a projection dimension of 192, the Vim model is trained via the Adam optimizer with a learning rate of 0.0001 and a batch size of 32. To prevent overfitting, validation loss

is monitored at each epoch, and an early stopping mechanism with a patience of 10 epochs is applied.

IV. EXPERIMENTAL RESULTS

This section discusses performance of the Vim model on our layout routing image dataset. Results from Vim are also benchmarked with those of transformer-based ViT and CNN-based DenseNet-121. Vim's training, validation and testing were performed on a Windows system featuring an Intel 2.1 GHz i7-14700 CPU, 16 GB of RAM and an NVIDIA RTX A4000 GPU.

A. Classification Problem

The classification task acts as a fast filter to identify layouts meeting specific performance thresholds, eliminating non-compliant designs without the computational expense of exact calculations. Verified compliant designs then proceed to the regression model for precise performance prediction and further optimization.

The model's classification performance is evaluated using metrics such as Accuracy, Precision, Recall and F1 score, which are defined as

$$\text{Accuracy} = \frac{\text{TP} + \text{TN}}{\text{TP} + \text{TN} + \text{FP} + \text{FN}}, \quad (1)$$

$$\text{Precision} = \frac{\text{TP}}{\text{TP} + \text{FP}}, \quad (2)$$

$$\text{Recall} = \frac{\text{TP}}{\text{TP} + \text{FN}}, \quad (3)$$

$$\text{F1} = \frac{2 \times \text{Precision} \times \text{Recall}}{\text{Precision} + \text{Recall}}, \quad (4)$$

where TP, TN, FP, FN are true positive, true negative, false positive, and false negative values, respectively.

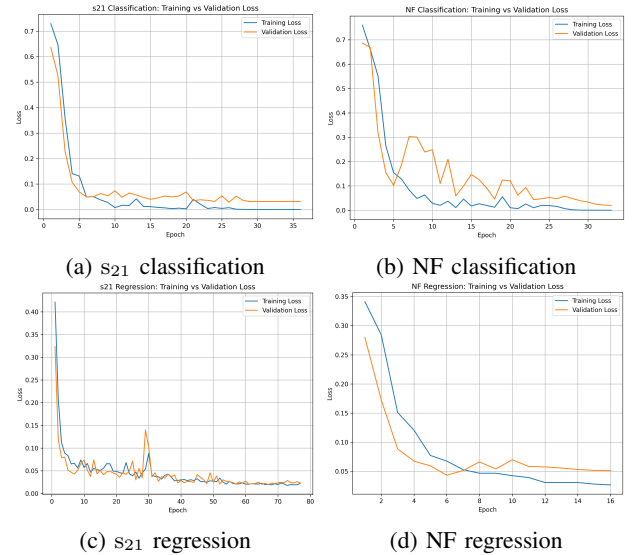


Fig. 4: Vim model's training versus validation loss

Fig. 4a and 4b compare the classification training and validation loss of s_{21} and NF. In both figures, training losses decline steadily toward zero, while validation losses converge to their final values of 0.0313 for s_{21} and 0.0201 for NF. This close alignment between training and validation trajectories confirms Vim's robust learning and effective generalization for the classification task.

Table I evaluates the Vim model's testing performance versus ViT and DenseNet-121 as two other established models. While DenseNet-121 achieves the overall highest accuracy,

TABLE I: Performance and Computational Efficiency Comparison on the Testing Set of Different Models for Classification Problem

Metrics	S ₂₁			NF		
	Vim	ViT	DenseNet-121	Vim	ViT	DenseNet-121
Accuracy (%)	95.57	94.69	98.23	97.35	95.57	97.2
Precision (%)	95.74	97.72	96.07	100	97.78	98.21
Recall (%)	93.75	89.58	100.00	93.75	91.67	96.49
F1 score	0.947	0.93	0.98	0.968	0.95	0.97
Training epochs	36	26	30	33	21	31
Training time (minutes)	87	148.2	217.5	79.8	119.7	224.8

recall and F1 score, Vim provides a more optimal balance of performance and speed. Notably, Vim achieves 100% precision in NF classification, outperforming both benchmarks. Crucially, Vim demonstrates superior computational efficiency across both tasks; it completes training in 87 minutes for S₂₁ and 79.8 minutes for NF, making it consistently 1.5 to 1.7 times faster than ViT and nearly three times faster than DenseNet-121. This performance empirically supports the architectural advantages of Vim, illustrating that the transition from self-attention mechanism to bidirectional SSM maintains the necessary modeling power while achieving subquadratic-time computation for high-fidelity layout filtering.

B. Regression Problem

To ensure faster and more stable convergence, z-score standardization is applied to the S₂₁ and NF values (dB scale). This transformation is defined as

$$z = \frac{x - \mu}{\sigma}, \quad (5)$$

where z is the standardized value, x is the original raw value, μ and σ are the mean and standard deviation of the dataset, respectively. Applying this scaling transforms the raw data into a standardized distribution with $\mu = 0, \sigma = 1$.

The evaluation metrics including mean absolute error (MAE), root mean squared error (RMSE) and R^2 are chosen with the given formulas below

$$MAE = \frac{1}{n} \sum_{i=1}^n |\hat{y}_i - y_i|, \quad (6)$$

$$RMSE = \sqrt{\frac{1}{n} \sum_{i=1}^n (\hat{y}_i - y_i)^2}, \quad (7)$$

$$R^2 = 1 - \frac{\sum_{i=1}^n (\hat{y}_i - \bar{y})^2}{\sum_{i=1}^n (y_i - \bar{y})^2}, \quad (8)$$

where y_i is the actual value, $\hat{y}_i$ is the predicted value of y_i and $\bar{y}$ is the mean value of all y_i in the dataset.

Fig. 4c and 4d compare the regression training and validation loss of S₂₁ and NF, respectively. The regression training and validation loss curves demonstrate rapid, stable convergence for both metrics. For S₂₁, training loss drops to 0.0192 by epoch 77, with validation loss closely following at 0.0234. NF regression converges even faster, reaching a training loss of 0.0264 and validation loss of 0.0610 within just 16 epochs. This consistent alignment across both tasks confirms the model's robust learning capacity and its ability to generalize effectively for precise layout performance regression.

TABLE II: Performance and Computational Efficiency Comparison on the Testing Set of Different Models for Regression Problem

Metrics	S ₂₁			NF		
	Vim	ViT	DenseNet-121	Vim	ViT	DenseNet-121
MAE (dB)	1.4	1.57	0.23	0.67	0.66	0.71
RMSE (dB)	2.1	2.45	0.32	1.25	1.31	1.26
R ²	0.97	0.96	0.98	0.92	0.9	0.88
Training epochs	77	45	40	16	38	35
Training time (minutes)	186.1	256.5	290	38.7	216.6	253.8

Table II demonstrates that while DenseNet-121 achieves the lowest error metrics for S₂₁ regression, Vim delivers a competitive R^2 of 0.97. Regarding NF regression, Vim achieves a superior R^2 of 0.92, outperforming both ViT (0.9) and DenseNet-121 (0.88). Notably, Vim's training efficiency for S₂₁ is striking, which is 1.38 times and 1.56 times faster than ViT and DenseNet-121. For NF training, Vim's 38.7-minute is even more impressive, which is approximately 5.5 times and 6.5 times faster than ViT and DenseNet-121. These results underscore how Vim's SSM-based structure can match or exceed the modeling power of both transformer-based ViT and CNN-based DenseNet-121 while drastically reducing the computational overhead for layout performance estimation.

The proposed Vim model achieves an inference time of less than 1 second, representing a massive speedup compared to approximately 4 minutes required for a standard industrial flow (including DRC, LVS, parasitic extraction and post-layout simulation) [18], [27]. While data generation requires a one-time computational investment, the trained model enables real-time performance estimation, eliminating the post-layout verification and simulation bottleneck to facilitate rapid, iterative layout optimization.

V. CONCLUSION

This study evaluates the Vim architecture for RF layout performance prediction. Our work utilizes a specialized dataset of 1,132 unique LNA layouts, represented through 21-channel routing and via layers, to benchmark bidirectional SSMs versus transformer-based ViT and CNN-based DenseNet-121. Instead of ViT's self-attention or DenseNet-121's localized kernel, our SSM-based methodology achieved a superior balance between modeling power and computational efficiency. Across both classification and regression tasks for S₂₁ and NF, Vim consistently demonstrated significant training speed advantages, outperforming ViT and DenseNet-121 benchmarks by up to 6.5 times. These findings confirm that Vim's SSM-based architectures with subquadratic-time complexity provide a highly scalable solution for reducing the computational overhead and accelerating the design cycle in RF layout performance prediction.

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